

A Systems Approach to Solder Joint Fatigue in Spacecraft Electronic Packaging

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Differential expansion induced fatigue resulting from temperature cycling is a leading cause of solder joint failures in spacecraft. Achieving high reliability flight hardware requires that each element of the fatigue issue be addressed carefully. This includes defining the complete thermal-cycle environment to be experienced by the hardware, developing electronic packaging concepts that are consistent with the defined environments, and validating the completed designs with a thorough qualification and acceptance test program. This paper describes a useful systems approach to solder fatigue based principally on the fundamental log-strain vs log-cycles-to-failure behavior of fatigue. This fundamental behavior has been useful to integrate diverse ground test and flight operational thermal-cycle environments into a unified electronics design approach. Each element of the approach reflects both the mechanism physics that control solder fatigue, as well as the practical realities of the hardware build, test, delivery, and application cycle.

Introduction

Mechanical fatigue of electronic component solder joints is an important failure mechanism that must be dealt with carefully in any high reliability electronic packaging design. Spacecraft electronic hardware is particularly vulnerable because the opportunity seldom exists to repair or rework the hardware after launch. The one-of-a-kind build philosophy, the vacuum-thermal environment of space, and the restriction to the use of only Hi-Rel components, also place important constraints on the selection of various electronic packaging approaches, and assembly and test procedures.

Figure 1 shows an example solder joint fatigue failure that occurred during ground testing of JPL's Magellan spacecraft electronics (Ross, 1989). The pictured lead is associated with a Dual Inline Package (DIP) integrated circuit mounted using a planar surface mount to allow the opposite side of the printed wiring board (PWB) to be bonded directly to the supporting chassis heat-conduction surface. For compatibility with surface mounting, most integrated circuits are obtained and used at JPL in either flat-pack or DIP packages with the leads bent in the gull-wing configuration illustrated in Fig. 2. This lead configuration provides for a positive spacing between the part and the board and provides part-board strain relief in the plane of the board.

For most parts, adequate heat transfer is provided by heat conduction down the part leads to the solder pads and through the PWB to the heatsink web. However, for high-power-dissipation parts, supplementary heat transfer paths must often be provided in parallel with the part leads. Such paths generally

involve filling the gap between the part and the board with a high-thermal-conductivity heat transfer material such as alumina or copper. Figure 3 illustrates the application of copper heat conductors under high-dissipation DIP packages. A historical problem with this heat-sinking approach is that the DIP package does not provide any lead flexibility in the normal-to-the-board direction to accommodate the thermal expansion of the heat-conduction spacer; this creates a high stress configuration that is particularly vulnerable to fatigue of the solder joints during temperature cycling.

With complex part mounting concepts such as these, achieving high-reliability long-life spacecraft electronics requires that each factor in the fatigue of solder joints be understood thoroughly and addressed systematically. Important elements in-



Fig. 1 Cracked solder joint of DIP in spacecraft electronics caused by expansion of clear Solithane in space between DIP and PWB

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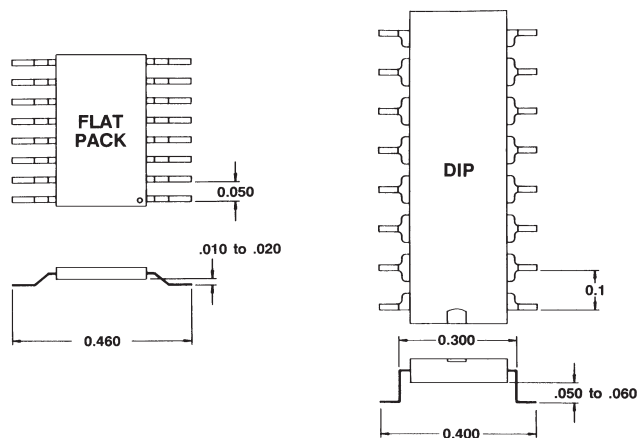


Fig. 2 DIP and Flat-pack electronic part packages with leads bent for surface mounting

clude careful definition of the complex fatigue environment to be experienced by the hardware, development and fabrication of electronic packaging concepts that are consistent with the defined requirements, validation of the completed designs with a thorough qualification and acceptance test program, and communication of the fatigue endurance limitations of the hardware to mission operations personnel. Each of these elements must reflect both the mechanism physics that control solder fatigue as well as the practical realities of the hardware build, test, delivery, and application cycle.

Solder Reliability Physics Overview

Before describing the systems approach being used to control solder failure at JPL, it is useful to first review the fundamental physics underlying the nature of solder failure—particularly the controlling parameters and their sensitivities. Considerable research has taken place over the last several years that has both illuminated the generic issues of mechanical failure of solder, and highlighted the unique and complicated properties of solder as an engineering material (Lau and Rice, 1985, and Lau, 1991).

In general, solder is a reasonably forgiving and tolerant material with a desirably low melting point that makes it ideal for making electrical attachment to parts that are compatible with modest processing temperatures. Because of its wide application and acceptance, this discussion is limited to the so-called near-eutectic (63-37 and 60-40) tin-lead solder that has a melting point of approximately 183°C.

Solder Metallurgical Considerations. Before exploring the mechanical properties of room-temperature solder, it is important to note that molten solder is an extremely good solvent, and readily dissolves metals such as copper and gold that it comes in contact with. Although this contributes to good surface wetting properties, the strength and ductility of solder, as with most metals, are strongly affected by small concentrations (1 to 5%) of contaminating elements (Berg and Hall, 1979). This makes solder-joint strength quite sensitive to the purity of the resulting solder in the joint, which is very dependent on the surface metals of the joint and the length of time the metals were exposed to molten solder during the soldering process. For the purposes of this paper it is assumed that good soldering practices are employed to minimize the contaminant levels—this includes removing gold plating in a pre-soldering tinning operation, and employing fast soldering operations with high purity solder. It is also assumed that good surface wetting is achieved.

Upon solidification from the melt, solder is composed of a matrix of lead-rich and tin-rich grains that give solder its granu-

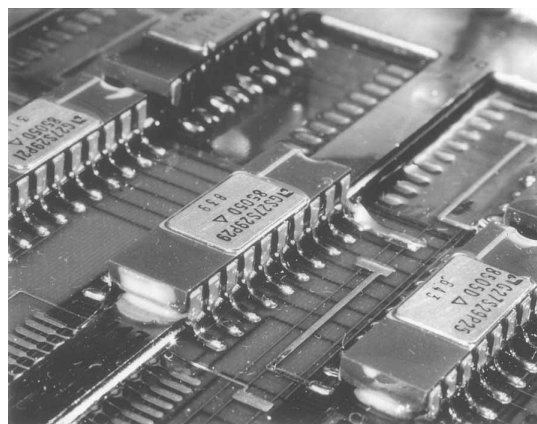


Fig. 3 DIPs mounted over 0.060" copper heat sinks

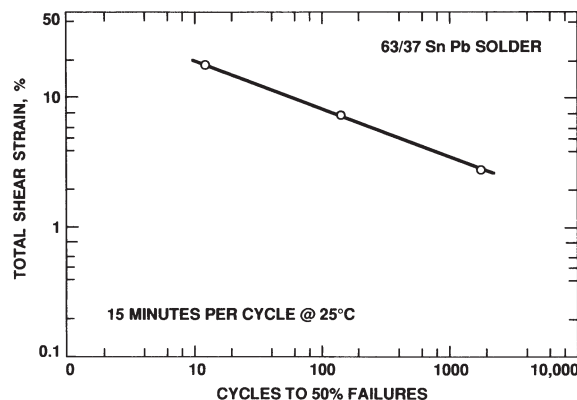


Fig. 4 Solder-joint fatigue life versus cyclic strain range (IBM data from Wild, 1975)

lar structure. Because the equilibrium concentration of tin and lead in the grains is a strong function of temperature, the chemical composition of the solder grains is determined by the cooling rate during solidification and the aging time following solidification. Interdiffusion between the grains over time also leads to growth of the size and spacing between the grains. The size and chemical composition of the solder's granular structure is very important because it has orders of magnitude effects on the ability of solder to creep under load. Lampe (1976) has found that these solder aging processes approach equilibrium in a matter of a few days at 100°C, or a few months at room temperature.

Solder Fatigue Strength. For most electronic packaging applications it is not a single high stress event that breaks a component solder joint; rather it is repeated load applications that result in fatigue failure of the solder.

Figure 4 presents representative fatigue-life data for 63-37 SnPb solder taken from IBM test results (Wild, 1975). The plot illustrates the typical dependency between cycles-to-failure and the level of total plastic strain introduced into the solder (total peak-to-peak strain range per cycle). Note that the level of damage (number of cycles to failure) is an extremely strong function of the cyclic strain range. Doubling the strain range can reduce the fatigue life by nearly an order of magnitude. This linear log-strain-versus-log-cycles-to-failure dependency is characteristic of ductile metals (Mon and Ross, 1982, and Aldrich and Avery, 1970), and is quite independent of temperature. Figure 5 presents data from Solomon (1986) illustrating the temperature independence of the solder fatigue properties measured under various isothermal conditions.

In most electronic packages, the principal strain in solder joints

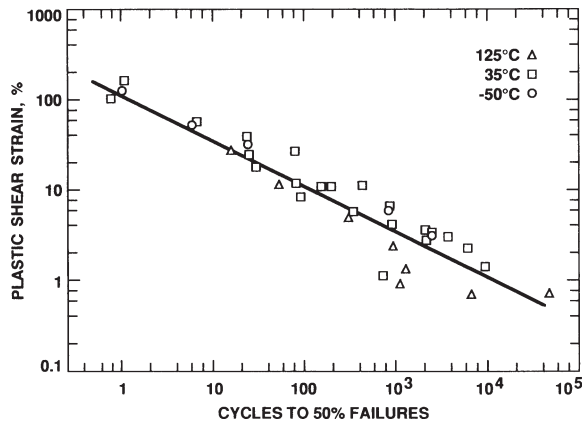


Fig. 5 Fatigue endurance of 60-40 solder versus solder temperature (from Solomon, 1986)

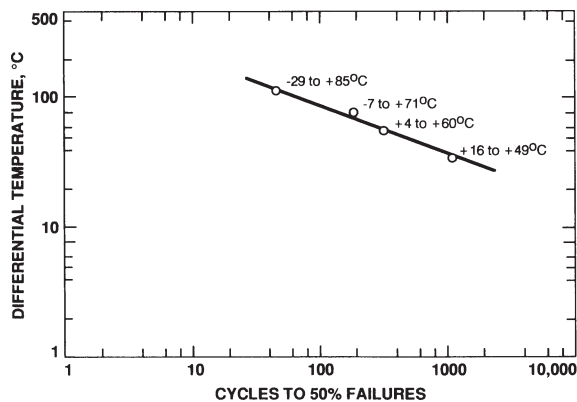


Fig. 6 Example solder-joint fatigue life versus temperature cycle depth for Solithane encapsulated parts (from TRW, 1983)

is caused by differential expansion between the part and its mounting environment due to changes in temperature (thermal cycles) and/or due to temperature gradients between the part and the board. For those cases where the strain is linearly dependent on the temperature swing, solder joint fatigue test data can also be conveniently plotted as cycles-to-failure versus temperature swing (ΔT). Figure 6 presents example temperature-cycle data gathered by TRW (1983) on actual electronic circuit board solder joints; note that these data exhibit the same characteristic log-log slope for solder as the IBM data in Fig. 4.

Creep-Fatigue Interactions. In general, the level of strain introduced by temperature cycling is under the control of the packaging engineer who determines the degree of part/board differential expansion matching, and/or the level of strain relief achieved using strain-relief elements such as the flexible metal leads of the electronic components. The function of strain relief elements is to lower the differential-expansion induced loads (stresses) on the solder joints to levels below the solder yield strength, thus minimizing the generation of plastic strain. Unfortunately, under typical application loading conditions the solder joints can still be expected to undergo modest levels of strain due to creep of the solder in response to the applied elastic forces from the strain relief elements. This creep induced strain has the same damaging effect as more immediately induced plastic strain, and must be directly summed with the plastic strain to achieve the total strain that is correlated with fatigue life in Fig. 4. Because of creep effects, the total strain range during any given loading cycle can be a strong function of solder temperature, the loading time per cycle, the applied solder stress, the spring con-

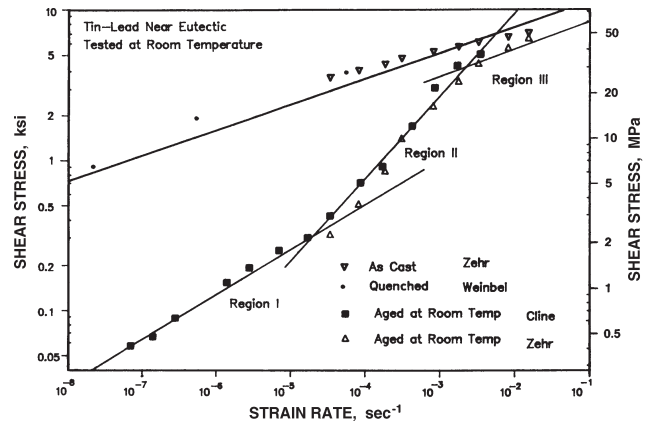


Fig. 7 Strain rate versus stress for Sn-Pb 63-37 solder at room temperature

stant of the strain relief elements, and the chemical composition and size of the solder grains. Figure 7 illustrates the strong sensitivity of solder strain rate (creep rate) to the solder stress resulting from the load applied by the electronic part/board system (including elastic strain relief elements) during the loading cycle (Cline and Alder, 1967, Weinbel et al., 1987, and Zehr and Backofen, 1968); also included is the sensitivity to the heat treatment condition of the solder. Upon examination, it is apparent that Fig. 7 describes both plastic strain and creep strain as a continuum, with plastic strain associated with the high strain rate (right-hand) end of the plot, and creep strain associated with the remainder of the plot. Although Fig. 7 is for room-temperature solder, the strain (creep) rate for a given applied stress can be extrapolated to other temperatures by noting that creep rate increases by a factor of approximately 1.8 for each 10°C increase in temperature (Kashyup and Murty, 1981).

Figure 7 is extremely useful for assessing the rough magnitude of creep effects likely to be encountered in any given solder loading application. For example, these data indicate that a constant 1 ksi (6.9 MPa) stress (less than $1/4$ the yield stress) will result in a 10% strain in less than an hour at room temperature with aged solder, and indicate that freshly made solder joints might be expected to creep significantly less. Extrapolating the data to elevated temperatures suggests that under the same 1 ksi (6.9 MPa) loading condition, a 10% strain would be reached in, for example, less than a minute at 100°C .

Figure 8, computed from the data of Fig. 7, highlights the cycle-rate dependency of creep that would be induced during square-wave displacement cycling of electronic components with typical elastic strain relief elements. In this case the stiffness of the strain reliefs was selected to limit the maximum solder stress to 1 ksi (6.9 MPa) prior to creep relaxation, and the cycle displacement (maximum stress relief deflection) was chosen to correspond to a maximum solder strain of 10% (when the solder stress totally relaxes to zero). The implication of these data is that creep related strain—and in particular the time, temperature, and elastic-stiffness dependency of creep—must be carefully factored into the design and testing of solder joints and component mounting techniques over a very broad range of cyclic frequencies.

In recent work by this author (Ross et al., 1991) finite-element creep simulation analyses have been used together with accelerated thermal cycle testing to quantify the creep-fatigue performance of a variety of common electronic part lead configurations, and to assess the implications of differing cyclic loading and temperature-cycling extremes. As might be expected, the analyses indicate that the strain relief afforded by elastic leads has important benefits in reducing the solder strain range during rapid cycling or during short-term temperature excursions to below 0°C , but has much less effect for typical application environ-

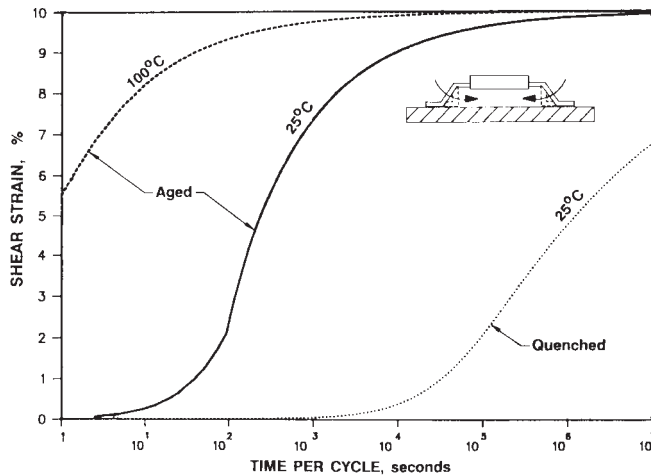


Fig. 8 Dependence of solder strain on cyclic loading period for joints with strain reliefs and part motions that limit the maximum solder stress to 1 ksi (6.9 MPa) and maximum solder strain to 10 percent

ments with multi-hour cycles at room temperature and above. This is because the solder joints of common part lead configurations—such as J-leads, DIPs, and Flat-packs—completely creep-relax at room-temperature and above in less than an hour. Thus, for this important class of room-temperature applications, the total solder displacement equals the part-board differential expansion associated with a given temperature change, i.e. the total solder strain range is directly proportional to the thermal-cycle temperature excursion. A useful implication for this class of applications having complete creep relaxation is the ability of the linear log-cycles-to-failure versus log- ΔT relationship illustrated in Fig. 6 to be used for fatigue-life characterization.

In contrast, for applications that involve rapid cycling or below-zero temperatures, lead stiffness and cyclic rate can have a significant effect on the developed strain range. For these applications, the relationship between strain range and ΔT , as embodied in the curve in Fig. 6, must be carefully determined for the cycle time, lead stiffness, and temperatures of interest.

Solder Fatigue Environmental Requirements

With the above background in the failure physics of solder, the first step in achieving high-reliability spacecraft electronics is to determine and understand the mechanical stress environment that the solder joints must survive. This must include all stressful environments from the moment the solder joints solidify, to the end of the space mission. For JPL spacecraft, the principal stressing environments are temperature-cycling induced differential expansion loads, and launch vibration induced loads. In general, vibration induced loads are small in comparison to the differential-expansion induced loads and will not be considered here.

To understand the thermal cycle exposure of flight hardware, JPL has extensively audited several recent missions including the Galileo and Magellan spacecraft. Table 1 illustrates numbers, depths and high-temperature dwell times of the thermal-cycle environments seen by representative Magellan spacecraft electronics. This particular electronics is always on during the mission, and therefore only sees very small ($\sim 3^\circ\text{C}$) temperature fluctuations about its room-temperature operating environment. However, during ground testing, the electronics is typically turned on and off each day to avoid the cost of around-the-clock personnel that would otherwise be required to monitor the operating flight hardware; this results in the cycles categorized as on/off testing. The oven curing category includes thermal exposures associated with curing various adhesives and conformal coating

Table 1 Example Thermal-Cycle Exposure for Magellan Flight Electronics

Cause of Temp Cycles	Temp Cycle Depth ($^\circ\text{C}$)	Number of Temp Cycles	Typical Maximum Temp ($^\circ\text{C}$)	High Temp Dwell Time (hours)
Thermal Qual Tests	85	9	90	24
Elect. Qual Tests	65	8	80	16
S/C Thermal Tests	50	1	55	24
S/C Thermal Tests	40	1	45	24
Oven Curing	25	25	60	8
On/Off Testing	15	1075	40	8
Flight Mission	3	4000	30	4

materials and outgassing solvent residues during fabrication. Qualification tests, including special troubleshooting tests to evaluate the thermal and electrical performance adequacy of the hardware, invariably create the largest cycling depths. These exposures have dwell times of several hours at temperatures up to 90°C .

To develop a tractable requirement for electronic packaging design, it is desirable to reduce these diverse thermal-cycle environments to a single composite fatigue environment. For this we appeal to the log-cycles-to-failure-vs-log-strain plot included as Fig. 4. The slope of this curve is dominated by the fatigue properties of metals as described by the Coffin-Manson Law (Manson, 1965):

$$N^\alpha \Delta \epsilon = \text{Constant} \quad (1)$$

For our application, where creep allows complete stress relaxation during each cycle, $\Delta \epsilon$ is roughly proportional to ΔT over the range of typical operating temperatures. Thus, Fig. 4 can be reformatted in terms of ΔT as shown in Fig. 6. Although the x-y position of the curve in Fig. 6 is a function of the particular packaging design, the slope of the curve is dominated by the same fatigue properties of solder as described by Fig. 4, i.e.

$$N^\beta \Delta T = \text{Constant}, \quad \text{where } \beta \approx \alpha \quad (2)$$

Equation (2) allows (N_1) temperature cycles of a particular depth (ΔT_1) to be converted to an equivalent number (N_2) of cycles at another depth (ΔT_2).

Thus,

$$N_1^\beta \Delta T_1 = N_2^\beta \Delta T_2 \quad (3)$$

or

$$N_2 = N_1 (\Delta T_1 / \Delta T_2)^{1/\beta} \quad (4)$$

This is graphically illustrated in Fig. 9.

Table 2 displays the result of using equation (4) to convert each of the thermal-cycle environments of Table 1 to an equivalent number of cycles at an arbitrary baseline depth of 125°C . Assuming Miners law for the addition of fractional damage allows the contributing cycles to be summed to a single composite thermal-cycle fatigue environment for the end-to-end mission—in this case 9.82 cycles with a 125°C ΔT . The value of β used is that associated with Figs. 4 and 6.

This display of the individual elements of the total fatigue environment is particularly useful for identifying the most damaging environments to the hardware—in this case the qualification and on/off operational testing.

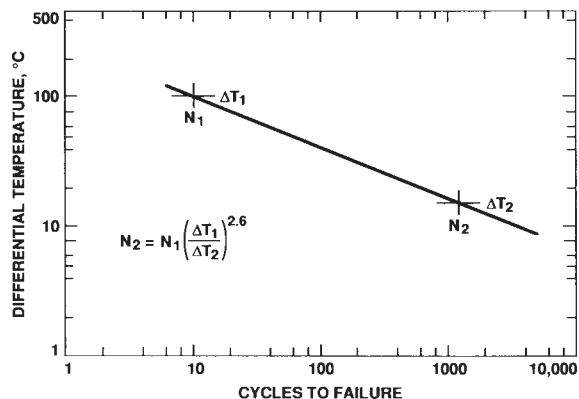


Fig. 9 Solder fatigue damage equivalence for various thermal-cycle depths

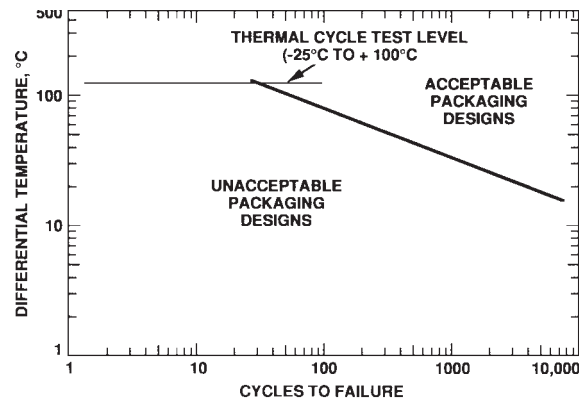


Fig. 10 Example solder-joint thermal-cycle fatigue-life requirement for spacecraft electronics

Table 2 Relative Severity of the Individual Elements of the Magellan Thermal-cycle Environment

Cause of Temp Cycles	Temp Cycle ΔT (°C)	Number of ΔT Cycles	Cycles* to Failure Ratio (125°C vs ΔT)	Equivalent Number of 125°C Cycles	Percentage Exposure per Environment
Thermal Qual Tests	85	9	0.367	3.30	33
Elect. Qual Tests	65	8	0.183	1.46	15
S/C Thermal Tests	50	1	0.092	0.09	1
S/C Thermal Tests	40	1	0.051	0.05	1
Oven Curing	25	25	0.015	0.38	4
On/Off Testing	15	1075	0.004	4.30	44
Flight Mission	3	4000	0.00006	0.24	2
TOTAL				9.82	100

$$* \text{ Ratio} = \frac{\text{Cycles for equal damage at 125°C}}{\text{Cycles at } \Delta T} = \left(\frac{\Delta T}{125} \right)^{2.6}$$

As a specification for the required fatigue endurance of electronic packaging, it is appropriate to multiply the total number of equivalent cycles computed for the end-to-end mission (e.g. the 9.82 number in Table 2) by a factor of 2 or 3 to provide margin for the statistical distribution of solder joint strengths. This leads to a qualifications test requirement such as that shown in Fig. 10, which corresponds to thirty 125°C cycles. Presentation of the fatigue requirements in this manner greatly improves communication among the broad range of involved personnel.

Qualification Testing and Inspection Issues

Once an electronic packaging design has been generated against the requirements of Fig. 10, or its equivalent for a particular mission, developmental tests are conducted at JPL on engineering mock-ups to validate the design approach for fatigue resistance. There are three critical issues in this effort.

- 1) The engineering mock-up must accurately duplicate the stress generating attributes and the solder strength properties of the flight hardware.
- 2) The accelerated environmental tests must accurately replicate, or bound in a worse-case sense, the total flight-hardware fatigue environment including the fabrication and ground-test environment.
- 3) The inspection approach must definitively establish the functionality or failure of the hardware.

Following successful qualification of the engineering-mock-up hardware, the actual flight hardware must also go through a thorough Qualification and Acceptance Test program. However, because fatigue is a wearout mechanism, these test programs are structured to test for electrical, thermal, and vibration load ad-

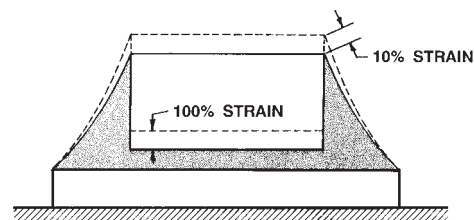


Fig. 11. Solder strain versus detailed joint geometry

equacy of the hardware, and are specifically designed to keep thermal fatigue to a minimum.

Engineering Mock-up Design Attributes. As noted in the Reliability Physics Overview the strength of solder joints is controlled by a number of very complex chemical and geometric aspects of the design. Specific issues include:

- 1) The purity of the solder in the joint is critically dependent on the metallurgy of the component leads and the dwell time that the solder is in the molten state. Dissolved contaminants and the formation of brittle intermetallic compounds drastically reduce solder strength.
- 2) The detailed geometry of the solder joint determines the level and distribution of strain in the solder for a given deflection of the electronic component. As shown in Fig. 11, key fillet areas may have order of magnitude lower strains and therefore many orders of magnitude greater fatigue endurance.
- 3) Features such as component leads that result in elastic loading of the solder joint not only reduce the immediate plastic strain resulting from imposed displacements, but also create longer-term creep loads with delayed effects. The effects of these elastic elements on fatigue is strongly tied to the stiffness (spring constant) of the individual elastic elements, the heat-treatment state and grain size of the solder, and the opportunity for creep (dwell time) in the loading environment.
- 4) The exact construction details of the flight article, including those introduced by rework processes and/or the application of conformal coating materials, can often lead to significantly altered solder-stress environments. An example is the Solithane conformal coating material that caused the fatigue failure pictured in Fig. 1.

Because of these issues, there is no substitute for designing and fabricating engineering test mock-ups as flight-like as possible. Particularly critical is the use of flight-like electronic packages that duplicate the metallurgy, geometry and stiffness of the flight component leads. At JPL, soldering and all other manufacturing steps are carried out using flight procedures, equipment, and personnel to the maximum extent possible.

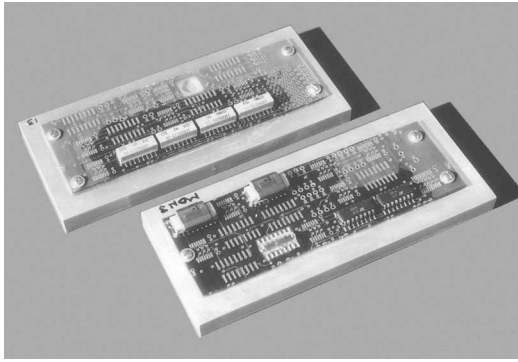


Fig. 12 Mock-up printed wiring boards used for thermal-cycle testing

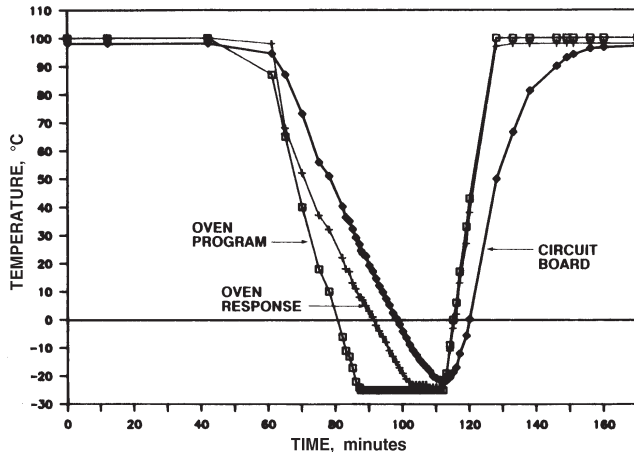


Fig. 13 Thermal cycle test environment used to characterize and qualify Magellan and Galileo solder joints

Figure 12 displays mock-up test boards manufactured using portions of flight PWBs bonded to aluminum flats that model the thermal expansion characteristics of the flight electronic chassis. Flight parts rejected for poor functional performance are mounted using flight processes and materials.

Accelerated Environmental Tests. Based on the typical fatigue environmental requirements illustrated in Tables 1 and 2, it is clear that, in addition to normal fatigue, creep-fatigue interactions can be expected to play an important role in the durability of JPL spacecraft solder joints. The facts that support this conclusion are the prolonged high temperature dwells associated with the temperature cycling environments and the elastic strain relief present in the leads of the gull-wing mounted DIPs and flat-packs. This implies that an accelerated test program must specifically address the demands and requirements of creep-fatigue testing, including possible pre-aging of the solder.

Cost effectiveness and engineering efficiency are other important test considerations; these argue for the shortest test possible, consistent with test accuracy, and therefore for high acceleration ratios. Test acceleration can be achieved in two ways—by increasing the temperature cycle rate, or by increasing the temperature cycle depth. The cycle extremes are constrained mostly by the demands for accuracy—in particular, it is prudent to neither exceed temperatures around 100°C, where solder and polymers start to lose physical properties quickly, nor drop significantly below temperatures such as -25°C, where solder achieves unrealistically low creep rates and high strengths, and where many otherwise soft polymers begin to pass well below their glass transition temperatures. For economic reasons it is

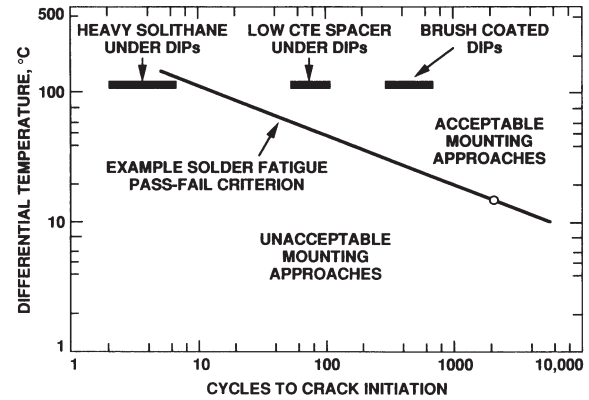


Fig. 14 Measured fatigue endurance of various DIP mounting approaches

also wise to stay within the capabilities of readily available thermal-cycle test chambers.

Following these arguments, a 3-hour-per-cycle thermal cycle profile from +100°C to -25°C was selected for testing of the Galileo and Magellan spacecraft electronics. This profile, shown in Figure 13, contains a long two-hour dwell at the 100°C level to achieve equilibrium creep in the solder joints, and to rapidly age the solder to its more vulnerable state. Because negligible creep occurs at -25°C, the dwell at this temperature is made just long enough to achieve thermal equilibrium. With this profile, a typical 100-cycle test requires a reasonable 2-week duration. Example results from this test procedure are displayed in Figure 14, contrasted with the example spacecraft environmental requirement previously shown in Fig. 10. Correlation of the test results with actual flight failures, such as that shown in Fig. 1, has been used to confirm the accuracy of the test levels and procedures.

Inspection Issues. In addition to the test article and thermal-cycle profile, inspection techniques and pass-fail criteria are also key elements of establishing the viability of a new packaging design. The nature of solder failure from a mechanical and electrical point of view is particularly important to understanding and developing inspection techniques and pass-failure criteria.

Under repeated application of plastic strain, the individual solder grains of a solder joint undergo both inter- and intra-grain distortion with the gradual development of microvoids along the grain boundaries. With continued straining, the microvoids gradually coalesce into microcracks, which in turn coalesce into larger cracks, eventually visible to the naked eye. Because the cracking is strain-induced, it occurs first in the region of the solder joint with the highest local strain. Unfortunately, in many practical solder joints, such as the joint shown in Fig. 11, this region is in the interior of the joint where it is obscured from external inspection. However, as the microcracks reach the surface of the shiny solder fillet they become relatively visible as localized regions with a frosty (non-specular) reflection. At JPL this is referred to as visible solder stressing or the presence of "stress". As the fatigue progresses, the visible stress becomes coarser in appearance and eventually, after cracking occurs, becomes more and more visible as a crack. Unfortunately, because an electronic component is held in place by many leads, cracks tend to remain tightly held together at room temperature. They can be extremely difficult to see, even by a trained eye at 50x, unless either: 1) the crack is mechanically held open, or 2) the crack is substantially burnished around the edges through repeated open-close cycles. This cyclically burnished crack is unlikely to be visible until sometime considerably after the original cracking occurs.

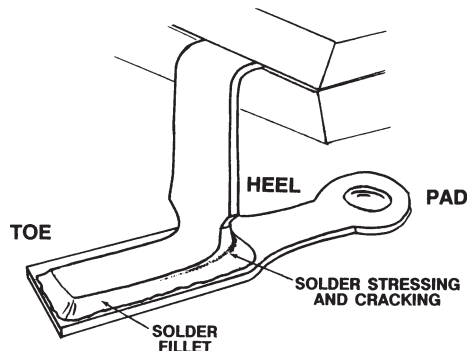


Fig. 15 Typical heel to toe crack propagation for gull-wing solder joints

It has been found that cracks are particularly visible and easy to see when mechanically held open while the break is still fresh and sharply defined. This situation has been found to occur when inspecting boards at elevated temperatures where the applied strain is at a maximum. Test boards have been found to be readily inspectable when withdrawn from thermal cycling at the maximum (100°C) temperature extreme. However, cracks that were readily visible at 100°C were often impossible to confirm after the board cooled to room temperature.

One of the strong advantages of the gull-wing solder joint used at JPL is that the normal fracture path is quite long and is highly visible during external inspection. As shown in Fig. 15, the fracture of this joint invariably originates at the heel and gradually progresses along the side fillets to the toe. Over an order of magnitude increase in cycling is required to cause modest signs of stress at the heel to propagate into a full fracture of the joint. This makes visual inspection of the joints quite viable, and has led to quantitative evaluation criteria based on the fraction of the length of the foot exhibiting stressing or cracking. A high quality stereo microscope at around 30x to 50x has been found to provide the most effective means for visually monitoring and quantifying solder joint health. Accurate assessments require carefully arranged viewing conditions with the microscope arranged approximately normal to the solder fillet surface. A movable semi-collimated light source is best to maximize the visibility of stress and cracking. Different styles of lighting are found to have a large effect on the ease of inspection.

Because questions sometimes arise in interpreting visual observations, mechanical pull tests have been conducted periodically to quantify the relationship between pull strength and the visual appearance of solder joints with various degrees of stressing. Good unstressed joints generally pull in the range of 4 to 8 pounds, with weaker joints in the 2 to 4 pound range. Joints that pull at 2 pounds or less are unacceptable for flight and generally correspond to ones that are visibly severely cracked.

One complication in the inspection process is the observation that solder joints on one side of an electrical component usually fail much more rapidly than those on the other side. This phenomena is related to the fact that as a solder joint fails, its overall strength decreases, and it therefore undergoes increasingly larger strains for a given applied load. With a typical multi-lead DIP or flat-pack, the loads and strains are initially equally shared by the two sides of the component. However, as the weaker of the two sides becomes evident, it begins to respond with a larger and larger fraction of the strain. This not only accelerates the fatigue of the weaker side, but physically unloads and retards the fatigue of the stronger side. The result is that one side of a part often fails totally, while the other side displays few if any visible signs of stress. The lesson, from an inspection point-of-view, is the need to always check the leads on both side of a part, and to

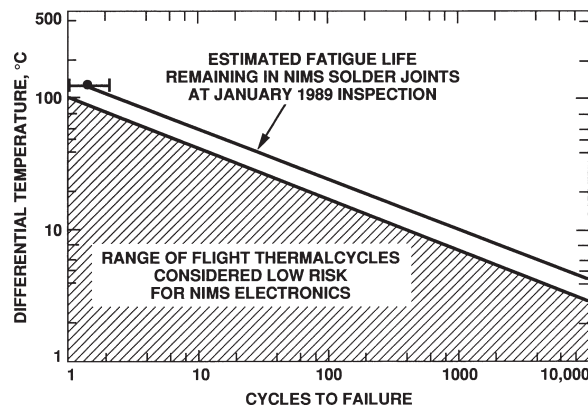


Fig. 16 Example communication of solder joint thermal-cycle exposure capability to mission operations personnel

disregard, from a statistics point of view, the leads on the good side.

Although the previous discussion has emphasized the visual-mechanical characteristics of solder fatigue, the electrical characteristics are just as important, and represent the ultimate criteria in terms of circuit board performance.

Unfortunately, electrical sensing of solder fatigue is just as troublesome as visual recognition. As a joint begins to fracture the first electrical signs are small micro-ohm increases in the electrical resistance of the solder joint. This resistance increase becomes proportionally larger with increasing numbers of fatigue cycles until fracture occurs; the total resistance increase at fracture is often on the order of 10%. Measuring these small resistance increases requires elaborate 4-wire measuring techniques and careful exclusion of temperature-induced resistance changes.

At the onset of fracture, the pattern of resistance increase changes to a series of short microsecond duration periods of high-resistance (> 200 ohms), similar to those encountered in a rubbing switch contact or potentiometer. As the fracture gradually burnishes with increasing cycles, the periods of high resistance increase in time and number until eventually a steady open circuit occurs. Although the steady open circuit is readily measurable it generally occurs only after two to five times the number of cycles required for the original fracture. To achieve an accurate estimate of the exact number of cycles to failure, Englemaier (1986) advocates the sensing of the short microsecond pulses immediately following fracture. Off-the-shelf electronics have become available for this application (Anatech, 1989), and it is currently being evaluated at JPL as part of our ongoing solder physics research. At this point, however, visual inspection coupled with the good inspectability and graceful failure trends of the gull-wing mount are the standard practice with JPL flight hardware.

Operational Considerations

A last short topic in the overall systems approach to solder fatigue is the use of fatigue theory to manage the end-use application of the delivered electronics so as to stay within its fatigue capabilities. In the ideal world this would be unnecessary because the environmental requirements discussed previously would be complete and accurate, and the mission would be proceeding according to its initial plan. In the real world, plans change and mission contingencies arise that can require revisiting the fatigue durability of flight hardware and mission risks after launch.

In this regard, the classical fatigue plot originally presented in Fig. 6 has the potential for yet another use—this time as a guideline for allowable mission thermal cycling. Figure 16 is a

representative example of the application of this concept to provide mission operations personnel with the data required to budget optimally the thermal-cycle exposure seen by some particularly vulnerable flight electronics over the life of the 5-year Galileo mission. The availability of such data plays a key role in allowing mission rewards and risks to be traded off in a knowledgeable and factual way.

Summary Remarks

Although solder fatigue is a complex subject with many unresolved issues, the level of understanding that has been developed over the past few years has made substantial progress in allowing fatigue resistant electronics to be designed and understood. The broad knowledge base that exists has allowed diverse ground test and flight thermal cycle environments to be integrated into unified requirements, and technically responsive qualification tests and inspection techniques to be identified. However, the growing diversity of part types, particularly the range of part size and lead strain relief, when coupled with the complex issues of creep-fatigue interaction, argue strongly for continued development and refinement of electronic packaging design and test techniques.

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